

ABSTRACT OF THE DISCLOSURE

The present invention relates to a method of forming interconnections for a temporary package, wherein the interconnections are capable of receiving solder balls on a die, partial wafer or wafer under test for testing and burn-in. The interconnections are formed in recesses sized and shaped to receive and contain approximately 10% to 50%, and preferably about 30%, of the total height of each solder ball within its associated interconnection. Such a design compensates for undersized or misshapen solder balls on the die under test and thereby prevents a possible false failure indication for the die under test. This design also distributes the forces on the solder ball caused by biasing the die under test to its temporary package to the periphery of the solder ball and thus reduces the likelihood of damage to the solder ball or the semiconductor substrate.

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